CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A method of fabricating a semiconductor device comprising the steps of:

providing a structure comprising a carrier wafer, an oxide layer positioned on the carrier wafer, a polySi back-gate located on the oxide layer, a back-gate dielectric located on said polySi back-gate, and a Si-containing layer located on said back-gate dielectric;

forming a channel region into a portion of said Si-containing layer;

forming a front gate region comprising a front-gate dielectric, a front polySi gate and sacrificial spacers atop said channel region;

forming undercutting shallow trench isolation regions in said structure;

removing the sacrificial spacers and forming source/drain extensions into the channel region; and

forming gate spacers atop the top of the channel region and source/drain regions in said channel region, wherein said polySi back-gate is self-aligned with the front polySi gate and the source/drain extensions.

2. The method of Claim 1 wherein said polySi back-gate is formed by implanting dopants into a polySi layer that is formed atop the back-gate dielectric and annealing the implanted dopants.

3. The method of Claim 1 wherein said back-gate dielectric is formed on the Si-containing layer of an initial silicon-on-insulator (SOI) substrate by a thermal growing process or deposition.

4. The method of Claim 1 wherein said bonded structure further includes deep trench isolation regions, each deep trench isolation region having an upper surface that is coplanar with an upper surface of the Si-containing layer.

5. The method of Claim 1 wherein said Si-containing layer of said bonded structure is thinned by a planarization process.

6. The method of Claim 1 wherein said bonded structure is formed by positioning said carrier wafer to be in contact with said oxide layer and performing a bonding step.

7. The method of Claim 6 wherein bonding step comprises heating at a temperature of from about 900° to about 1100°C for a time period of about 1.5 hours to about 2.5 hours.

8. The method of Claim 6 wherein said bonding step is performed at a temperature of from about 18° to about 27°C in the presence of an inert ambient.

9. The method of Claim 1 wherein said channel region is formed by ion implantation and annealing.

10. The method of Claim 9 wherein a sacrificial oxide layer is formed on the Si-containing layer prior to said ion implantation.

11. The method of Claim 1 wherein said sacrificial spacers have a width of from about 50 to about 100 nm.

12. The method of Claim 1 wherein said undercutting shallow trench isolation regions are formed by the steps of: chemical etching, isotropic reactive ion etching, oxidation and a second isotropic etch.

13. The method of Claim 1 wherein said sacrificial spacers are removed utilizing a chemical etchant.

14. The method of Claim 1 wherein said gate spacers are formed by deposition and etching.

15. The method of Claim 1 wherein said source/drain regions are formed by ion implantation and annealing using the gate spacers as an implant mask.

16. The method of Claim 1 further comprising forming raised source/drain regions on said source/drain regions, said raised source/drain regions are formed by deposition of an epi-Si or Si layer and ion implantation and annealing.

17. The method of Claim 16 further comprising forming silicide regions on said raised source/drain regions.

18. The method of Claim 17 further comprising forming an insulating layer having conductively filled contact holes atop the structure.